GENERAL INFORMATION

National Institute of Technology (NIT), Hamirpur HP, is organizing a short term course cum training programme on "Challenges and Opportunities in VLSI Design & Technology (COVDAT-14)" from 23.06.2014 to 27.06.2014.

Candidates admitted will be provided free lodging and boarding. These arrangements for all participants shall be made in NIT Hamirpur. Those participants not availing this facility will not be entitled to any rebate. Family accommodation is not available on campus. However, one may make his/ her own arrangement in city hotels at his/ her own expense. Candidates are requested to claim TA from their organizations.

OBJECTIVES OF THE COURSE

The conventional MOS device, which is the workhorse of VLSI technology, behaves different for smaller dimensions compared to its larger cousin. In recent years, new design constraints come up dictated by increased gate leakage, tunneling and the interconnects. These have led to different device configurations and geometries. Moreover, as silicon technology scales into the nanometer regime, the material set and device structures employed by the conventional field effect transistor (FET) are beginning to reach their limits. Currently, many critical device dimensions have reached 1 to 20 nm, and microelectronics is now on a transition to nano-electronics. Already, several architectures, such as fully depleted SOI, waferbonded double-gate and FinFET have been demonstrated with promising electrical characteristics at gate lengths of 25 to 10 nm. Thus new material and technology options need to be investigated for performance enhancement of electronics systems. The research in design and technology over the last few years has led to low power-high speed devices in the field of modern VLSI Era.

The aim of this programme is to provide an exposure in the emerging field of

VLSI devices and design to the participant. VLSI devices in nano scale have the intrinsic advantage to be most easily scalable to large numbers and integrable into electronic circuits.

COURSE CONTENTS

- Fundamental of MOSFET
- Semiconductor devices Modeling
- Novel devices for nanoelectronics
- Quantum Structure and Devices
- Nanoscale fabrication techniques
- Timing and power issues in Nano devices
- Nanoscale Memory Design
- Design Optimization Techniques
- Challenges in Nano Electronics
- EDA Tools

ELIGIBILITY: - The course is open to the teachers from the Networking Institutes, other technical institutes, Govt. organizations & personnel from industry

IMPORTANT DATES:

Last date for submission:	13-06-2014
Intimation of Acceptance:	14-06-2014

REGISTRATION AND FEE

Application in the prescribed format duly sponsored by the Head of the Institutution along with registration fee listed below in the form of a Demand Draft favoring "**Registrar, NIT Hamirpur**" payable at State Bank of India, NIT Hamirpur and must reach the Coordinator on or before 13th June, 2014.

Educational Institution	: Rs 500/-
Students PG/ PhD	: Rs 250/-
Industry Personnel	: Rs 1000 /-

APPLICATION FORM

Short Term Course on

Challenges and Opportunities in VLSI Design & Technology (COVDAT-14)

June 23 - 27, 2014

1.	Name of the applicant:
2.	Designation:
3.	Name of the Institute where Employed:
4.	Name of the Dept.:
5.	Official Mailing Address:
PIN	:
6.	Tel. No:
7.	Mobile No:
8.	Email id(must):
9.	Demand Draft Particulars
	Amount Rs: No: Date:
10.	Academic Qualification:
11.	Specialization:
12.	Experience in years:

Signature of the Applicant with date

Note: 1. Photocopied Reg. Form can be used or may be downloaded from institute website.

Sponsorship Certificate

We here by sponsor Dr./ Mr./Ms

participate in the STC on "**Challenges and Opportunities in VLSI Design & Technology** (**COVDAT-14**)". Further, I have personally talked to the applicant and he/she seemed to be sure to attend the course, in case the admission is offered to him/her.

Place: - -----

Date: - -----

Signature with Date & Seal

of Sponsoring Authority (Principal/ Director)

Address For Correspondence

After completion, Please mail this to:

Er. Vinod K. Sharma

Coordinator,

Short Term Course on (COVDAT-14) Deptt. of Electronics & Comm. Engg.

National Institute of Technology

Hamirpur -177005, H.P.

Phones: 01972	2-254644 (O)
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01972-254645 (R)

094180 26145(M)

Fax: 01972-223834

Email: ervinodsharma2003@gmail.com

ABOUT NIT HAMIRPUR HP

National Institute of Technology (NIT), Hamirpur is one of the seventeen NITs of the country, established in 1986 as a joint and cooperative enterprise of the Govt. of India and Govt. of Himachal Pradesh. It has been given the status of a Deemed University.

NIT is about 3 km from the Hamirpur bus stand, from where taxis and local buses are frequently available. Direct bus-service is available from Delhi, Chandigarh and all other important places. The nearest railway station is Una (HP) important religious places namely Jwalaji, Chintapurni, Deot-Sidh, Chamunda Devi & Brijeshwari Devi are an added attraction to the place.

Department of E&CE, NIT Hamirpur was pioneered in 1988. It has a high ranking in the North Region. The alumni/ students are well placed in TI, Motorola, ST Micro, SCL, DRDO, VSNL & the others.

The department has B.Tech. M.Tech. and Ph.D. Degree programmes.

COURSE COORDINATOR

Er. Vinod Kumar Coordinator, STC on COVDAT-14 Assistant Professor, Deptt. of E&CE, N.I.T. Hamirpur Hamirpur-177005 Himachal Pradesh Tel: 01972-254644(O), 254645(R), and 09418026145(M)

SHORT TERM COURSE

on

Challenges and Opportunities in VLSI Design & Technology (COVDAT-14) June 23 - 27, 2014

(Under TEQIP & SMDP-II) For Faculty/PG students of Technical / Govt. Institutes & Personnel from Industry

Patron

Prof. V.S. Ramamurthy Chairman BOG, NIT Hamirpur

Chairman Prof. Rajnish Shrivastava Director, NIT Hamirpur H.P

Co-Chairman Dr. Rajeevan Chandel HOD, E&CED, NIT Hamirpur H.P.

Coordinator

Er. Vinod Kumar



Organized by

Department of Electronics & Communication Engineering National Institute of Technology (NIT) Hamirpur Hamirpur -177 005 Himachal Pradesh, India

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